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**NORTH SOUTH UNIVERSITY**

**Department of Electrical and Computer**

**Engineering**

**Digital Logic Design (CSE 231)**

Faculty – Dr Mohammad Monirujjaman Khan(KMM)

Section: 06

Group: 04

**Project Part 3**

Sequential Part

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**CONTRIBUTION**

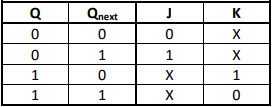
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| --- | --- |
| Work done By | Topic |
| Rasiqur Rahman Rifat | 1.Theory |
| Towsif Muhtadi Khan  (Coordinator) | 2.State Diagram |
| 3.State Table |
| Rafidul Islam | 4.K Map |
| 5.Combinationa Circuit |
| Towsif Muhtadi Khan ,Khalid Bin Shafiq, Rafidul Islam, Rasiqur Rahman Rifat | 6.Circuit diagram |
| Khalid Bin Shafiq | 7.555 Timer |

**Synchronous Sequential Circuits:**

Sequential Circuit is made of combinational circuits and memory storage where circuits conduct the operation of present output based on present inputs and past outputs stored in memory storage. In a sequential circuit, the values of the outputs depend on the past behavior of the circuit, as well as the present values of its inputs. A sequential circuit has states, which in conjunction with the present values of inputs determine its behavior. Sequential circuits can be Synchronous where flip-flops are used to implement the states, and a clock signal is used to control the operation.

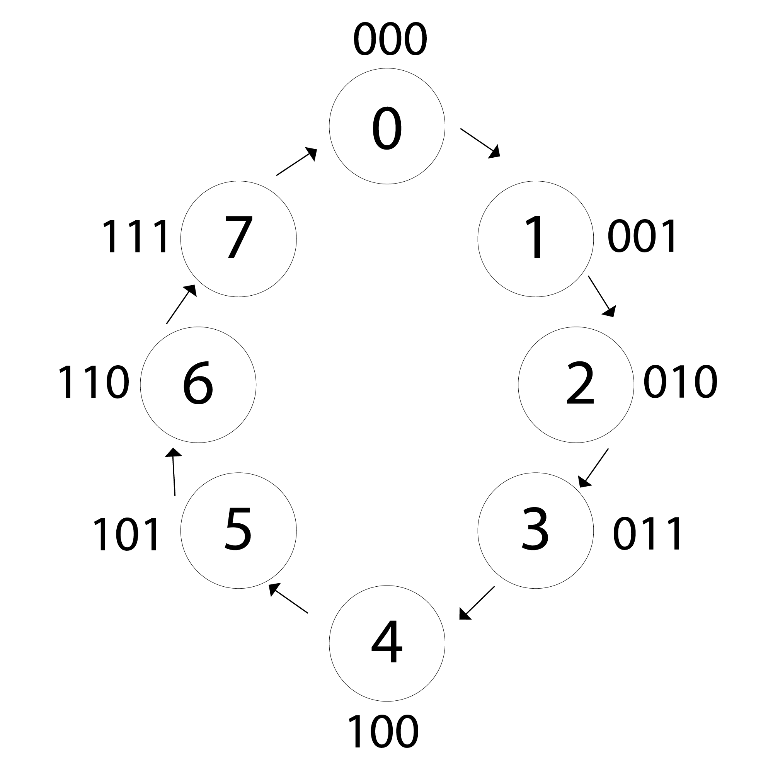
**JK Flip flop:**

A JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.



*JK flip-flop: Excitation Table*

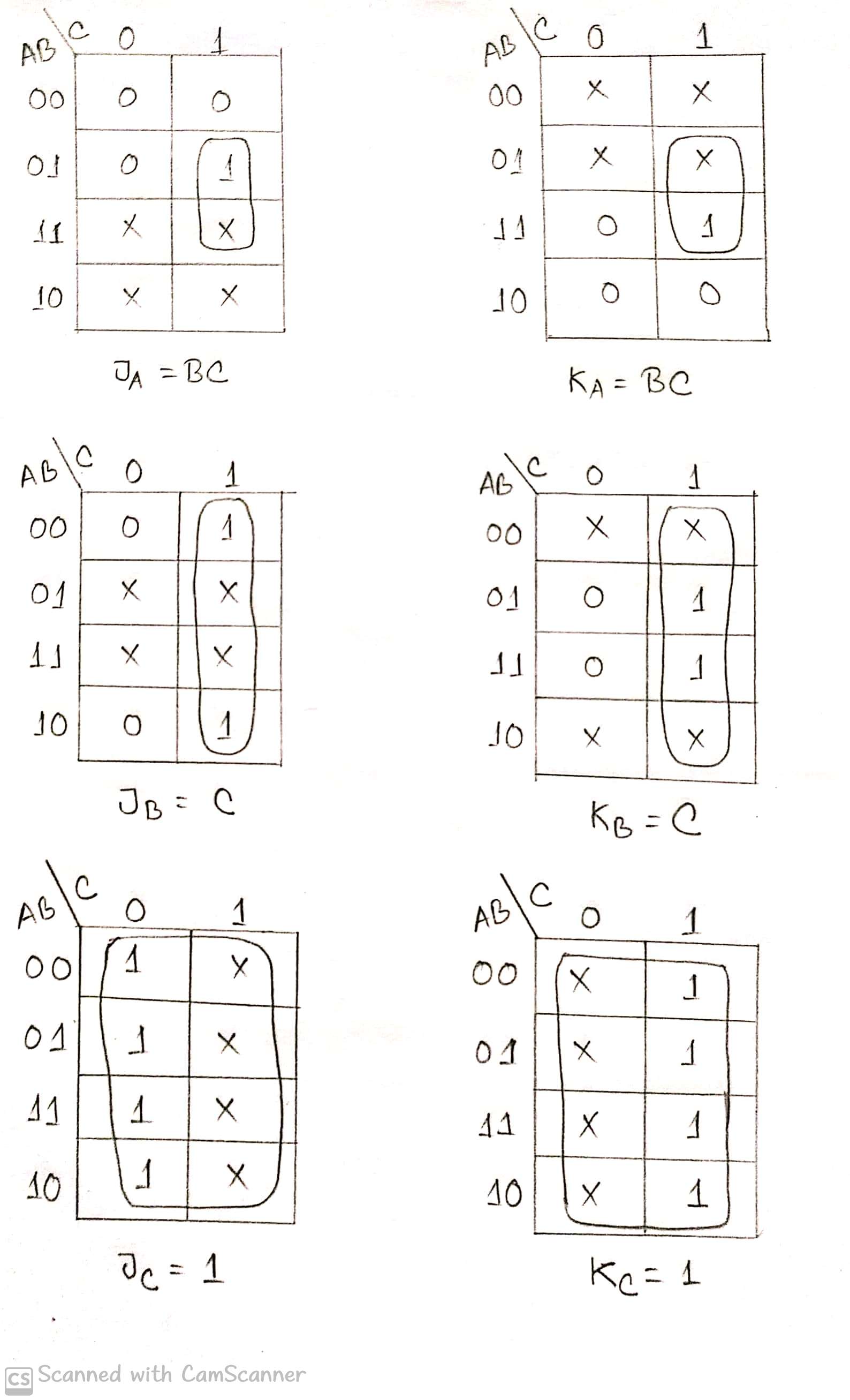
**The state diagram for our project (CSE-231) is:**



**State Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present state Input | | | Next stateOutput | | | Flip-flop input functions | | | | | | |
| A | **B** | **C** | **A** | **B** | **C** | | **JA** | **KA** | **JB** | **KB** | **Jc** | **Kc** | |
| 0 | 0 | 0 | 0 | 0 | 1 | | 0 | X | 0 | X | 1 | X | |
| 0 | 0 | 1 | 0 | 1 | 0 | | 0 | X | 1 | X | X | 1 | |
| 0 | 1 | 0 | 0 | 1 | 1 | | 0 | X | X | 0 | 1 | X | |
| 0 | 1 | 1 | 1 | 0 | 0 | | 1 | X | X | 1 | X | 1 | |
| 1 | 0 | 0 | 1 | 0 | 1 | | X | 0 | 0 | X | 1 | X | |
| 1 | 0 | 1 | 1 | 1 | 0 | | X | 0 | 1 | X | X | 1 | |
| 1 | 1 | 0 | 1 | 1 | 1 | | X | 0 | X | 0 | 1 | X | |
| 1 | 1 | 1 | 0 | 0 | 0 | | X | 1 | X | 1 | X | 1 | |

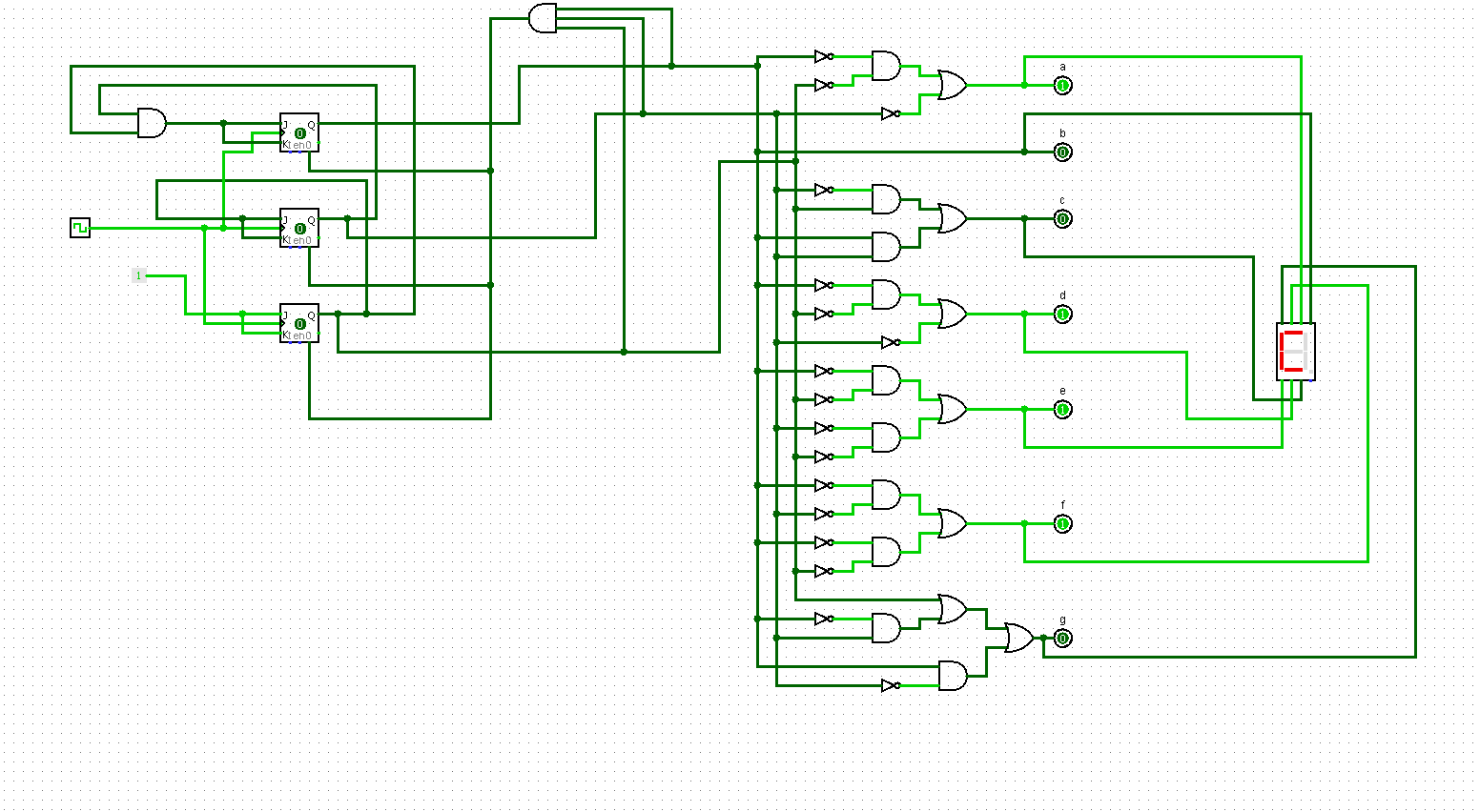
**Kamp:**

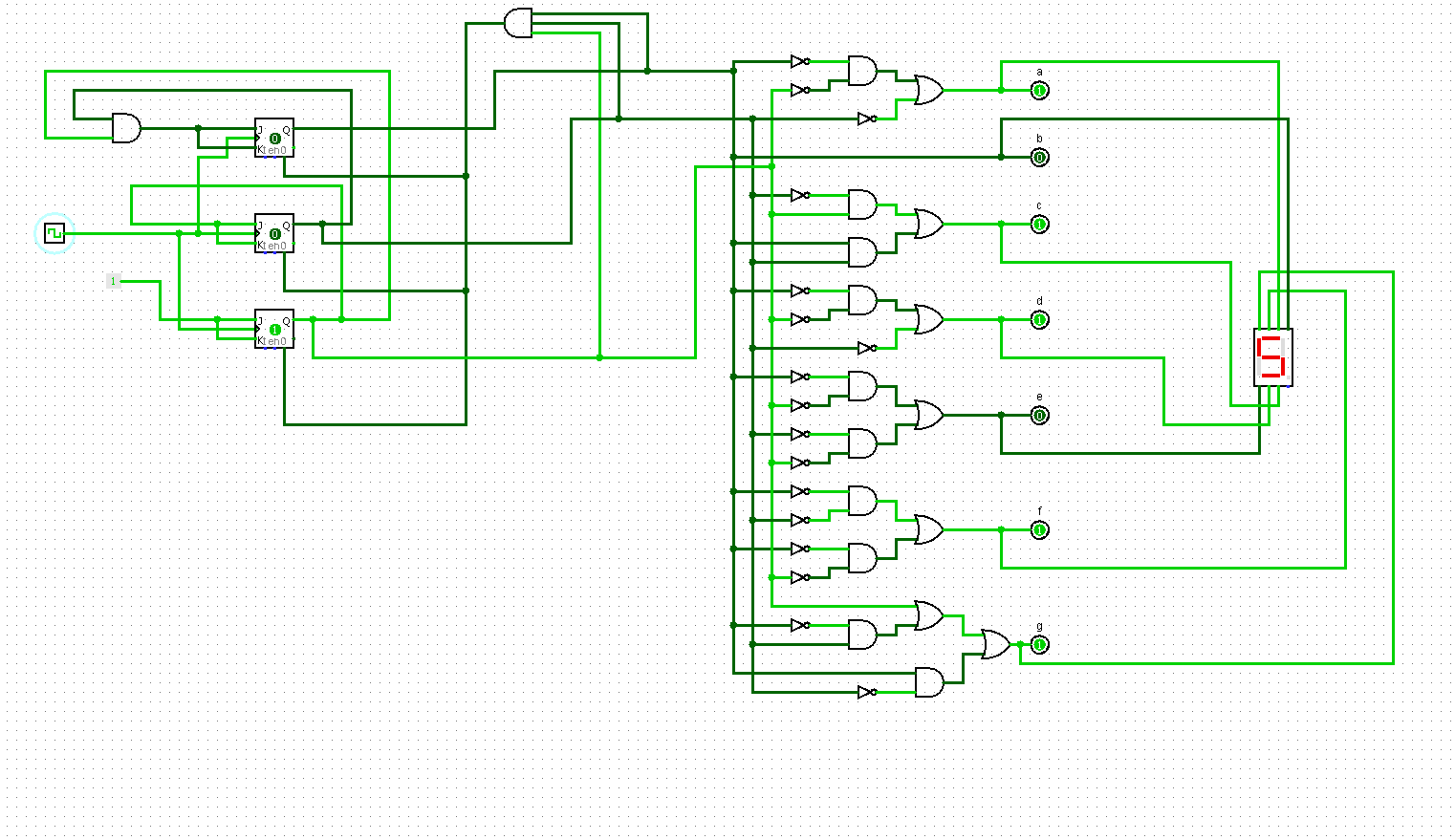


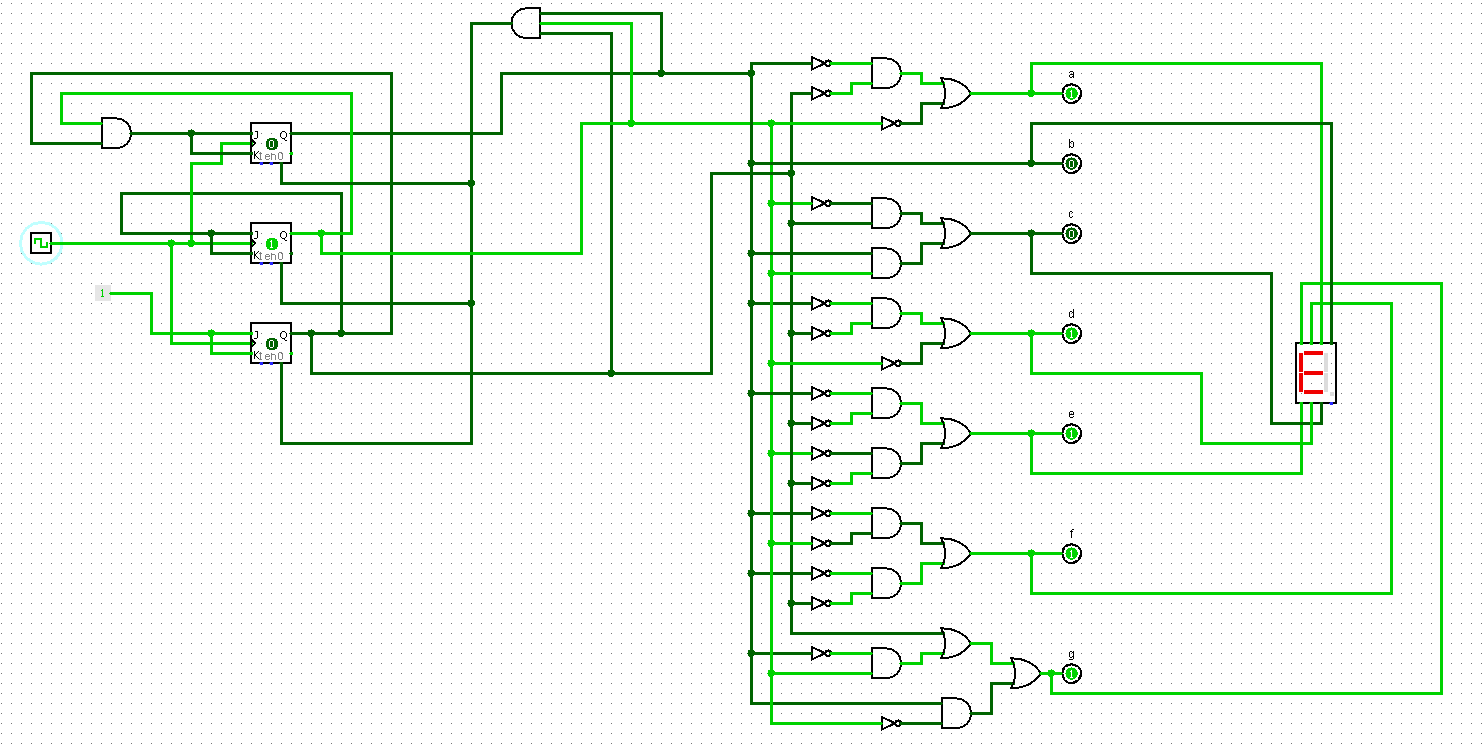
From the K map we get the following equations:

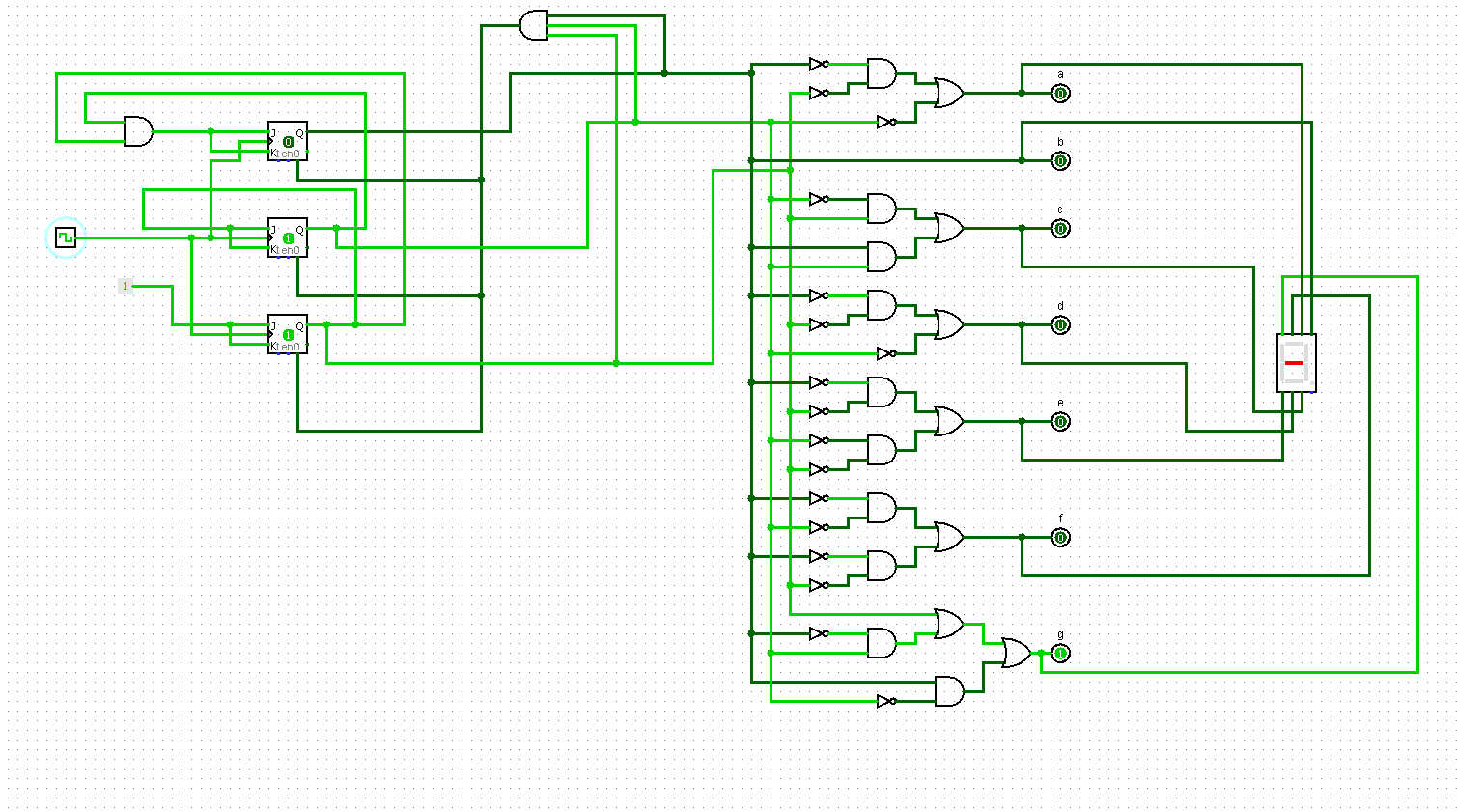
**JA**= BC **KA**=BC  **JB**= C  **KB**= C **JC**=1  **KC**=1

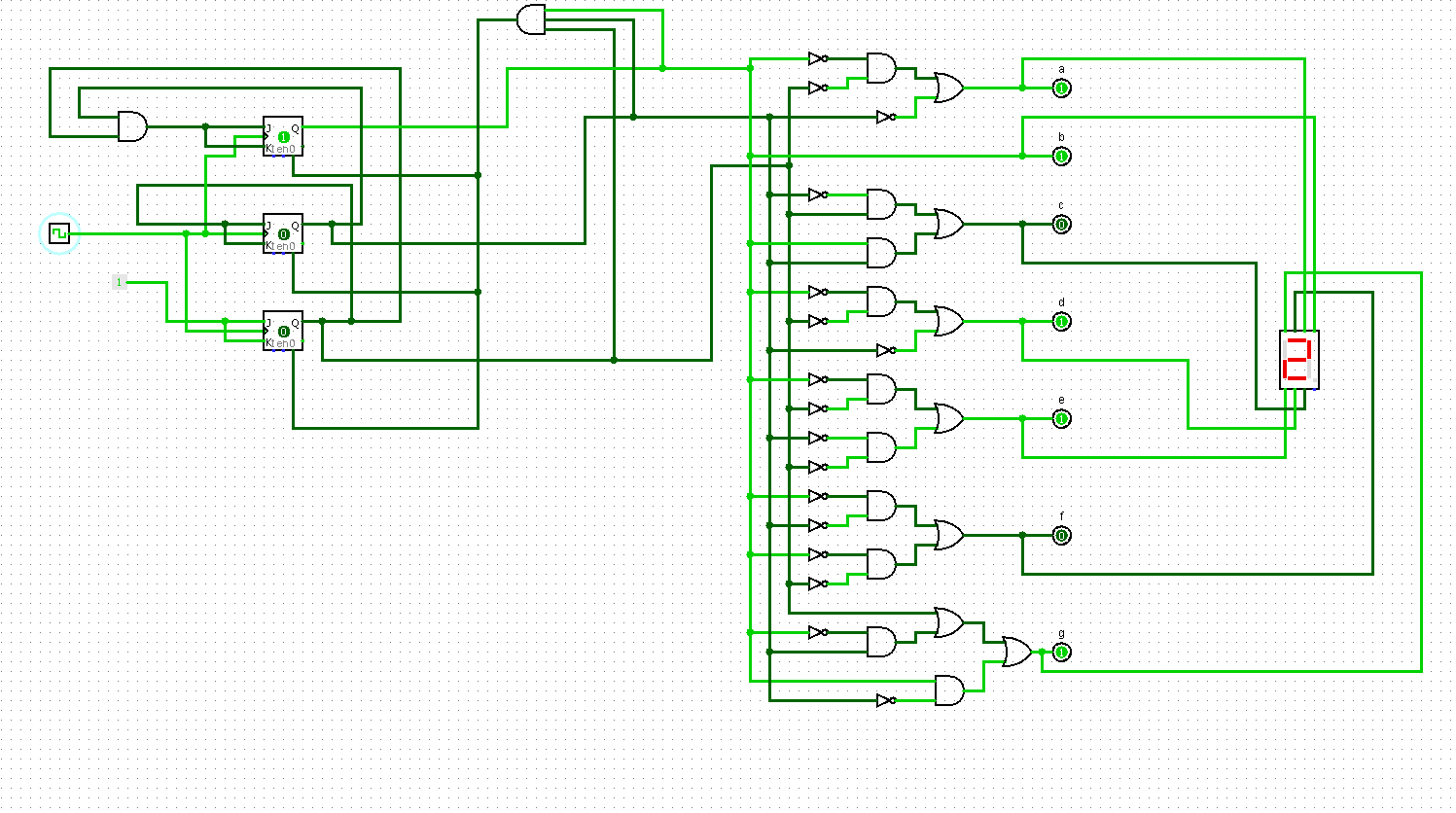
**Circuit Diagram for Sequential Part:**

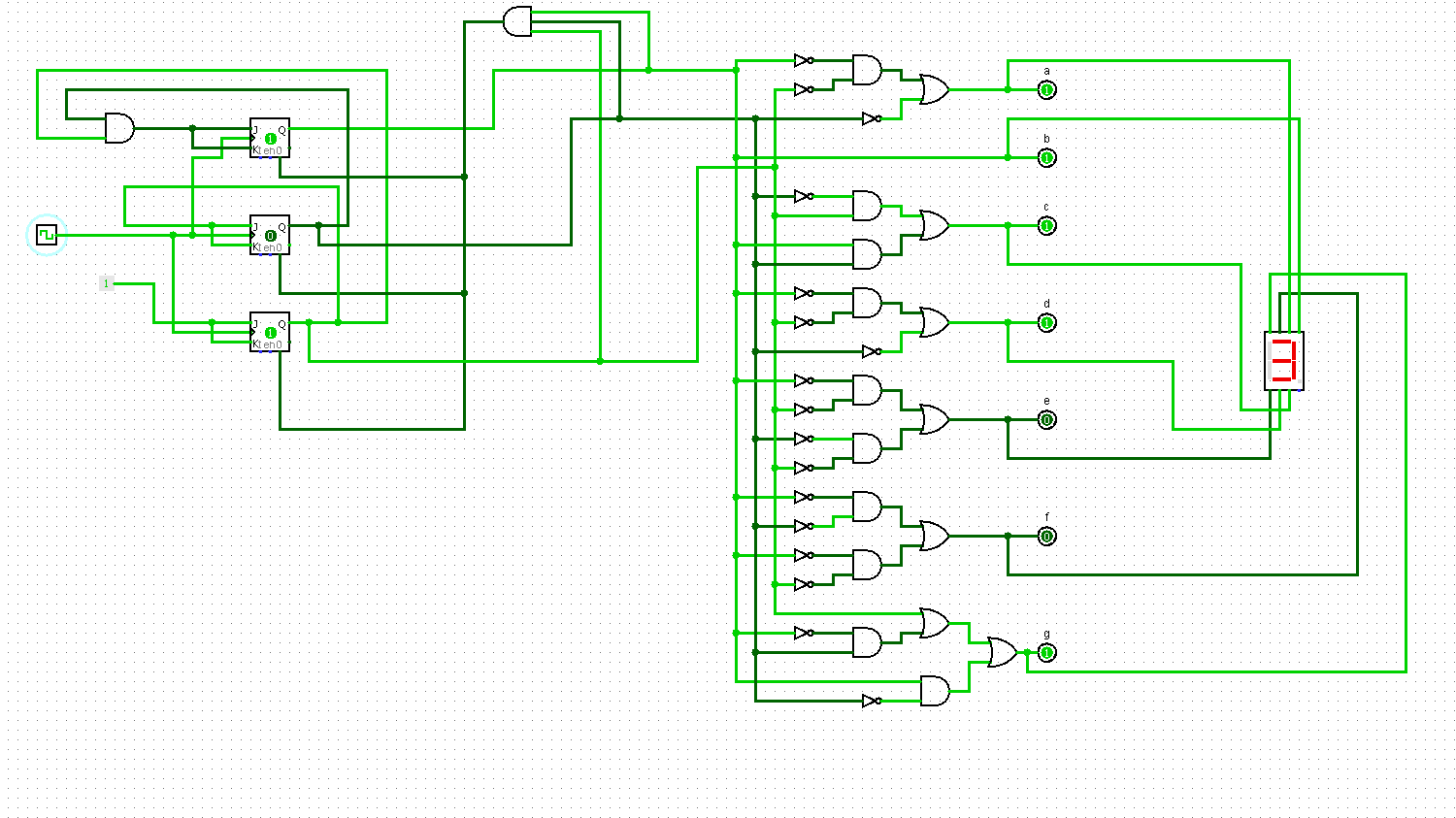
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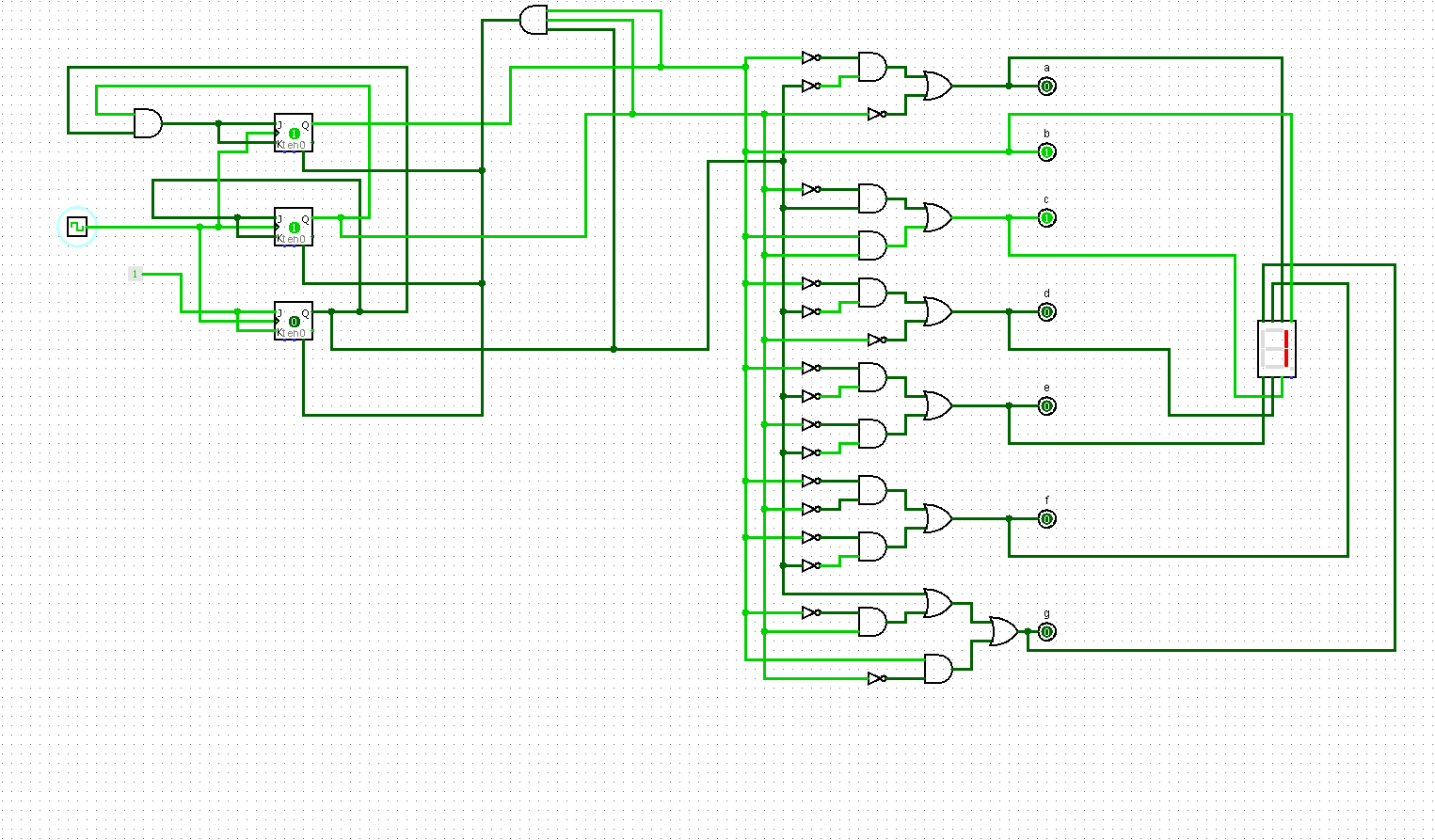
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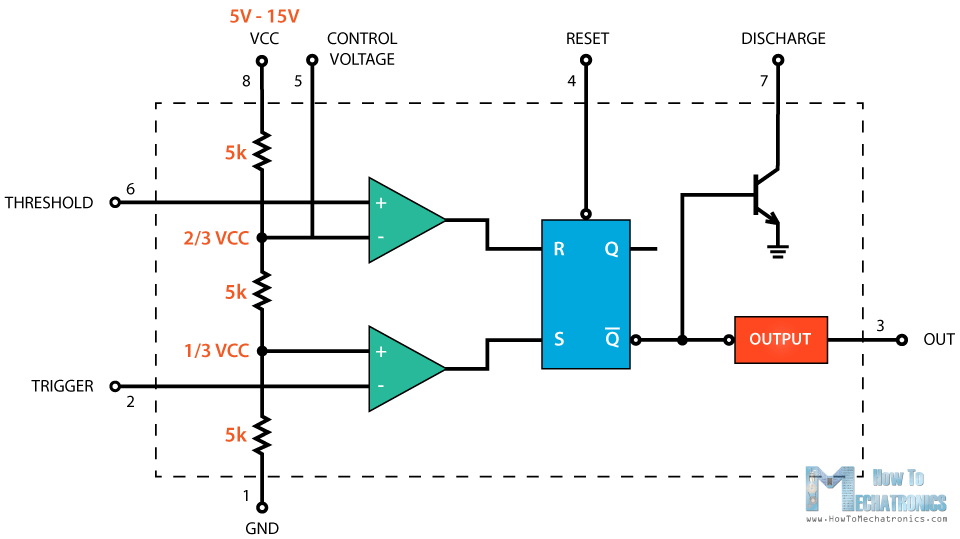
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**555 Timer:**

555 timers are integrated timing circuits which are used commonly as a source of clock pulses to drive subsequent timer circuits. They are analogue devices which can produce an oscillating and digital output. The IC can be configured to give an astable, period output or a monostable, single triggered output.



***Figure:*** *555 Timer*

This is the basic structure of a 555 timer represented with a block diagram it consists of 2 comparators, a flip-flop, a voltage divider, a discharge transistor and an output stage

The voltage divider consists of three identical 5k resistors which create two reference voltages at 1/3 and 2/3 of the supplied voltage, which can range from 5 to 15V.

Next are the two comparators. A comparator is a circuit element that compares two analog input voltages at its positive (non-inverting) and negative (inverting) input terminal. If the input voltage at the positive terminal is higher than the input voltage at the negative terminal the comparator will output 1. Vice versa, if the voltage at the negative input terminal is higher than the voltage at the positive terminal, the comparator will output 0.

The first comparator negative input terminal is connected to the 2/3 reference voltage at the voltage divider and the external “control” pin, while the positive input terminal to the external “Threshold” pin.

On the other hand, the second comparator negative input terminal is connected to the “Trigger” pin, while the positive input terminal to the 1/3 reference voltage at the voltage divider.

So using the three pins, Trigger, Threshold and Control, we can control the output of the two comparators which are then fed to the R and S inputs of the flip-flop. The flip-flop will output 1 when R is 0 and S is 1, and vice versa, it will output 0 when R is 1 and S is 0. Additionally, the flip-flop can be reset via the external pin called “Reset” which can override the two inputs, thus reset the entire timer at any time.

The Q-bar output of the flip-flip goes to the output stage or the output drivers which can either source or sink a current of 200mA to the load. The output of the flip-flip is also connected to a transistor that connects the “Discharge” pin to ground.

In our project we are showing “CSE – 231” sequentially through BCD to 7 segment display. For the sequential part we are using a JK Filp-flop. As we are using Logisim so we are using “Clock” to give a clock pulse. But if we use a 555 Timer then we can set e frequency and then “CSE-231” will be displayed sequentially in the display after a fixed time automatically.